CLAIMS

We claim:

1. A method comprising the steps of:

receiving a first clock signal;

providing a distributed clock signal to a clock distribution network having a plurality of endpoints connected to a respective plurality of components; and

modifying the distributed clock signal until a portion of the distributed clock signal received at a first end point of the plurality of endpoints is substantially synchronized to the first clock signal.

2. The method of claim 1, wherein the step of modifying includes providing a delayed representation of the distributed clock signal at the first end point.

3. The method of claim 2, wherein the step of modifying includes using a delay locked loop to modify the distributed clock signal.

4. The method of claim 3, wherein the first endpoint is at a same propagation level same level as a second endpoint of the clock distribution tree, where the second endpoint drives a component that is not part of the tree.

5. The method of claim 4 further including the steps of:

providing a second clock signal from a first device wherein the first clock signal is a delayed representation of the second clock signal.

6. The method of claim 5, wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path manufactured onto a first substrate, wherein the first substrate is not part of first the device.

7. The method of claim 6, wherein the step of receiving the first clock signal includes receiving the first clock signal at the first device.

8. The method of claim 5, wherein the step of receiving the first clock signal includes receiving the first clock signal at the first device.

9. The method of claim 3 further including the steps of:

providing a second clock signal from a first device wherein the first clock signal is a delayed representation of the second clock signal.

10. The method of claim 9, wherein the step of providing the second clock signal includes providing the second clock signal to a propagation path manufactured onto a first substrate, wherein the first substrate is not part of first the device.

11. The method of claim 10, wherein the step of receiving the first clock signal includes receiving the first clock signal at the first device.

12. The method of claim 9, wherein the step of receiving the first clock signal includes receiving the first clock signal at the first device.

13. A method comprising the steps of:

providing a first clock signal from a first device;

receiving a representation of the first clock signal from external the first device at the first device;

providing the representation of the first clock signal to a delay element;

providing a delayed clock signal from the delay element to a clock distribution tree, wherein the delayed clock signal is based upon the representation of the first clock signal, and the clock distribution tree includes a plurality of leaves that provide the delayed clock signal to a respective plurality of components;

providing a representation of the delayed clock signal from a first leaf to the delay element, where the first leaf is one of the plurality of leaves; and

modifying the delayed clock signal provided by the delay element based upon the representation of the delayed clock signal from the first leaf.

14. The method of claim 13, wherein the step of modifying the delayed clock includes modifying the delayed clock by delaying the first clock by an amount approximately equal to a first propagation delay and a second propagation delay, wherein the first propagation delay is equal to a delay along a delay path from the first device a second device, and the second propagation delay is equal to a delay along a delay path from the second device to the first device.

15. A method comprising the steps of:

generating a first clock edge at a first device at a first time, wherein first clock edge is associated with a first clock having a first period;

receiving the first clock edge at a second device at a second time, wherein the time between the first time and the second time is a first propagation delay;

generating a data signal a the second device at a third time in response to receiving the first clock edge, wherein the time between the second time and the third time is a second propagation delay;

receiving the data signal at a first component of the first device at a fourth time, wherein the time between the third time and the fourth time is a third propagation delay;

providing a representation of the first clock to a delay component of the first device, wherein the representation of the first clock is approximately equal to the first clock delayed by an amount approximately equal to the sum of the first, second and third propagation delays;

generating a distributed clock from the delay component to drive a clock distribution network having a plurality of endpoints;

receiving at the delay component a representation of the distributed clock at a first endpoint of the plurality of endpoints; and

modifying the distributed clock until the representation of the distributed clock at the first endpoint is synchronized with the representation of the first clock.

16. The method of claim 15 wherein the second device is a memory device.

17. The method of claim 15, wherein the first period is less than approximately 5 nanoseconds.

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18. An apparatus comprising:

a delay locked loop having a reference input, a feedback input, and a delayed reference output; and

a distribution network having a first node connected to the delayed reference output, and a plurality of end nodes connected to a respective plurality of components, a first end node of the plurality of end nodes connected to the feedback input of the delay locked loop, where the delay locked loop is one of the plurality of components.

19. The apparatus of claim 18 the distribution network is a clock distribution network.

20. The apparatus of claim 18 further comprising:

a first input port having an output node coupled to the reference input of the delay locked loop, and an input node, wherein the first input port, the distribution network, and the delay locked loop are formed on a first substrate; and

a first trace connected to the input node of the first input port, wherein the first trace is formed on the second substrate which is different than the first substrate; and

a first output port having an output node coupled to the first trace, wherein the output port is formed on the first substrate.

21. The apparatus of claim 20 further comprising:

a second output port having an output node connected to a second trace, wherein the second output port is formed on the first substrate, and the second trace is formed on the second substrate;

a second device having an input coupled to the second trace and an output coupled to a third trace, wherein the second device is formed on a third substrate which is different from the second substrate and the third trace is formed on the second substrate; and

a first input port having an input node connected to the third trace, and an output node coupled an input of one of the plurality of components.

22. The apparatus of claim 21, wherein the first trace is at least as long a the sum of the lengths of the second trace and the third traces.

23. A method comprising the steps of:

providing a first clock signal from a first device, wherein the first clock signal is transmitted over a first substrate to a second device, wherein the first substrate is not part of the first device or the second device;

providing a second clock signal from the first device, wherein the second clock signal is transmitted over a second substrate, wherein the second substrate is not part of the first device or the second device;

receiving the second clock signal at a delay component of the first device as a modified second clock signal;

receiving a third signal at a storage component, in response to the first clock signal, wherein the latching signal is based upon the modified second clock signal and a previous latching signal from the delay component; and

latching the third signal at the storage component based upon the latching signal.

24. The method of claim 23, wherein the latching signal is delayed from the modified second signal by an amount approximately equal to a clock period of the modified second clock plus a delay time between the latching signal being generated and the latching signal latching the third signal.